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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

A10

SOVP BUILD

2019.10.03

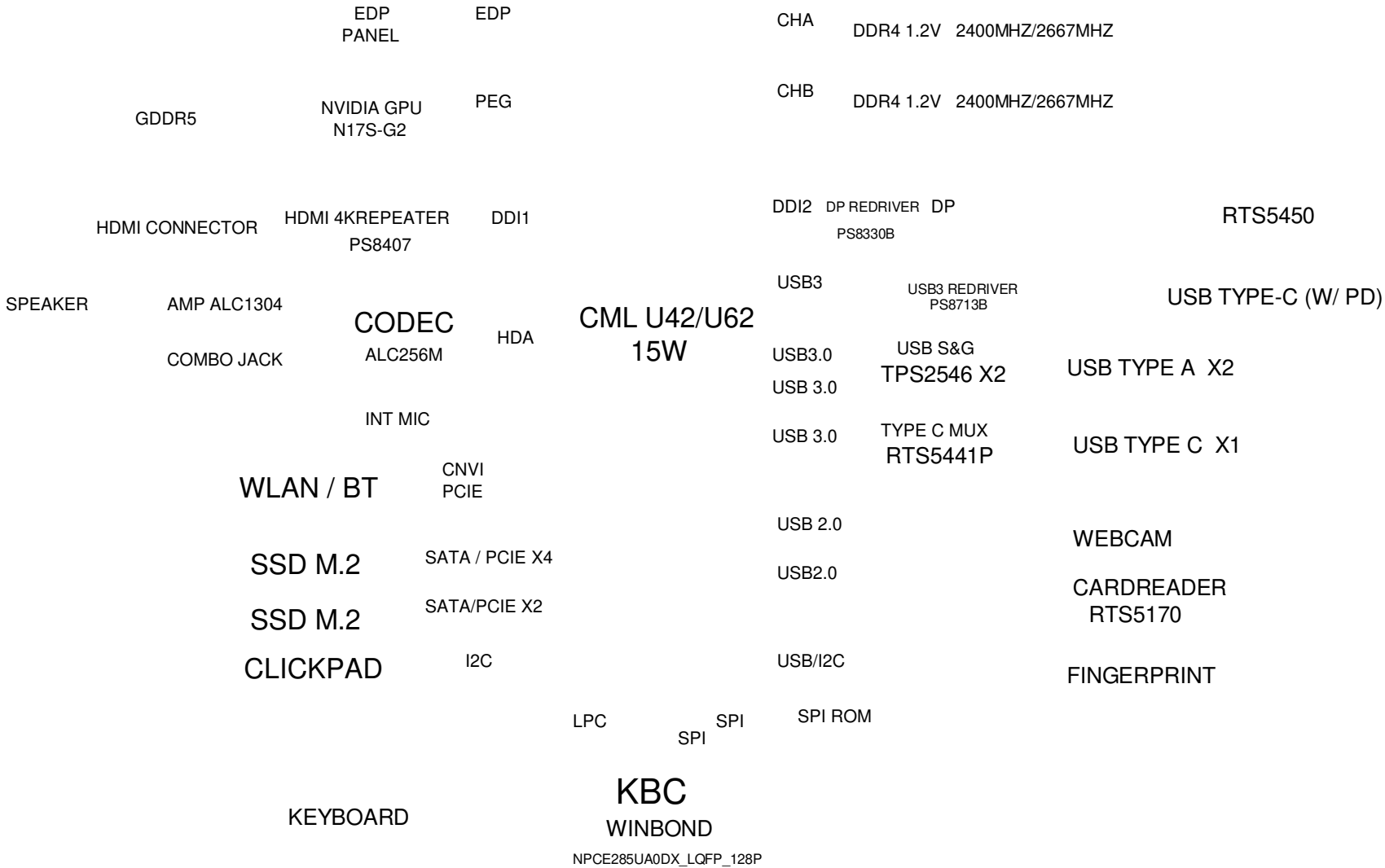
12-Apr-2019		
DATE	CHANGING	REV

DESIGN / DRAWER	XXX	DATE	12-Apr-2019
CHECK	BRYAN CHIOU		
APPROVAL	TUCKY TSAI		
FILENAME	R10_TOPAZ_WS		
PCB PIN	60xxxxxxxxxxx	PCB VER	X01

INVENTEC			
TITLE A10			
SIZE A1	COLOR G	DRAW NUMBER 1310xxxxx-0-0	REV X01
SHEET 1		of 20	

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CHARGER

DON'T PUT
ANY CAPACITOR

PVADPTR

DON'T PUT ANY CAPACITOR

SPECIAL CASE, PLEASE CHECK CN6050 PIN 1

INVENTEC

CHANGE by
PCB P/N XXXX
60xxxxxxxxxxx

DATE
PCB VER 12-Apr-2019
X01

TITLE
A10 Block Diagram
DOC NUMBER
1310xxxx-0-0
REV X01

REV
X01

SIZE
A3
CODE
CS
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C

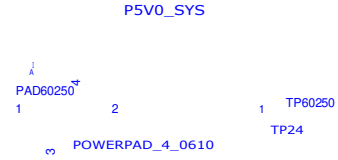
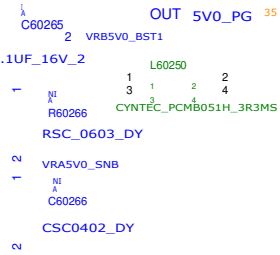
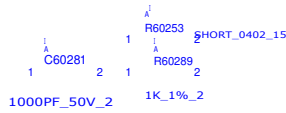
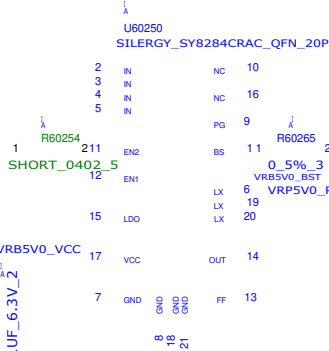
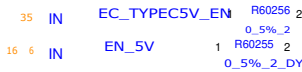
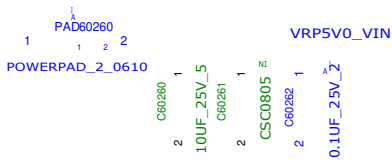


B



TITLE
A10 Block Diagram
SIZE CODE DOC.NUMBER REV
A3 CS 1310xxxxx-0-0 X01
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PVBAT



INVENTEC

[illegible]

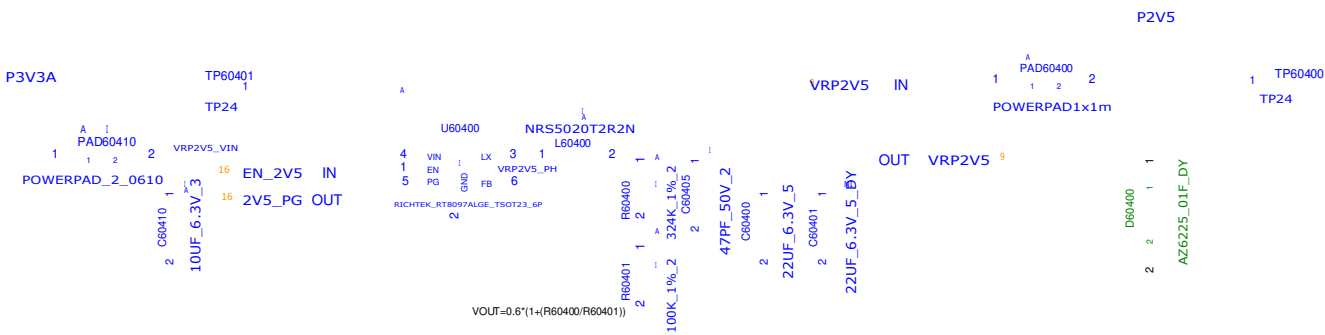
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SIZE CODE DOC.NUMBER
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CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 12-Apr-2019
PCB VER X01

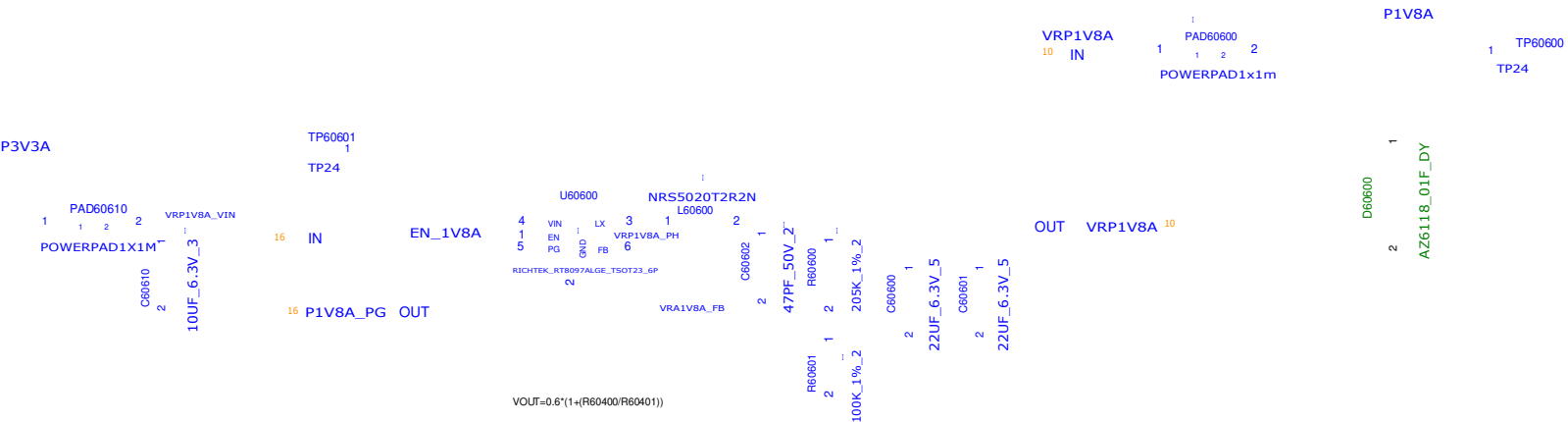
2 1

P2V5



INVENTEC

P1V8

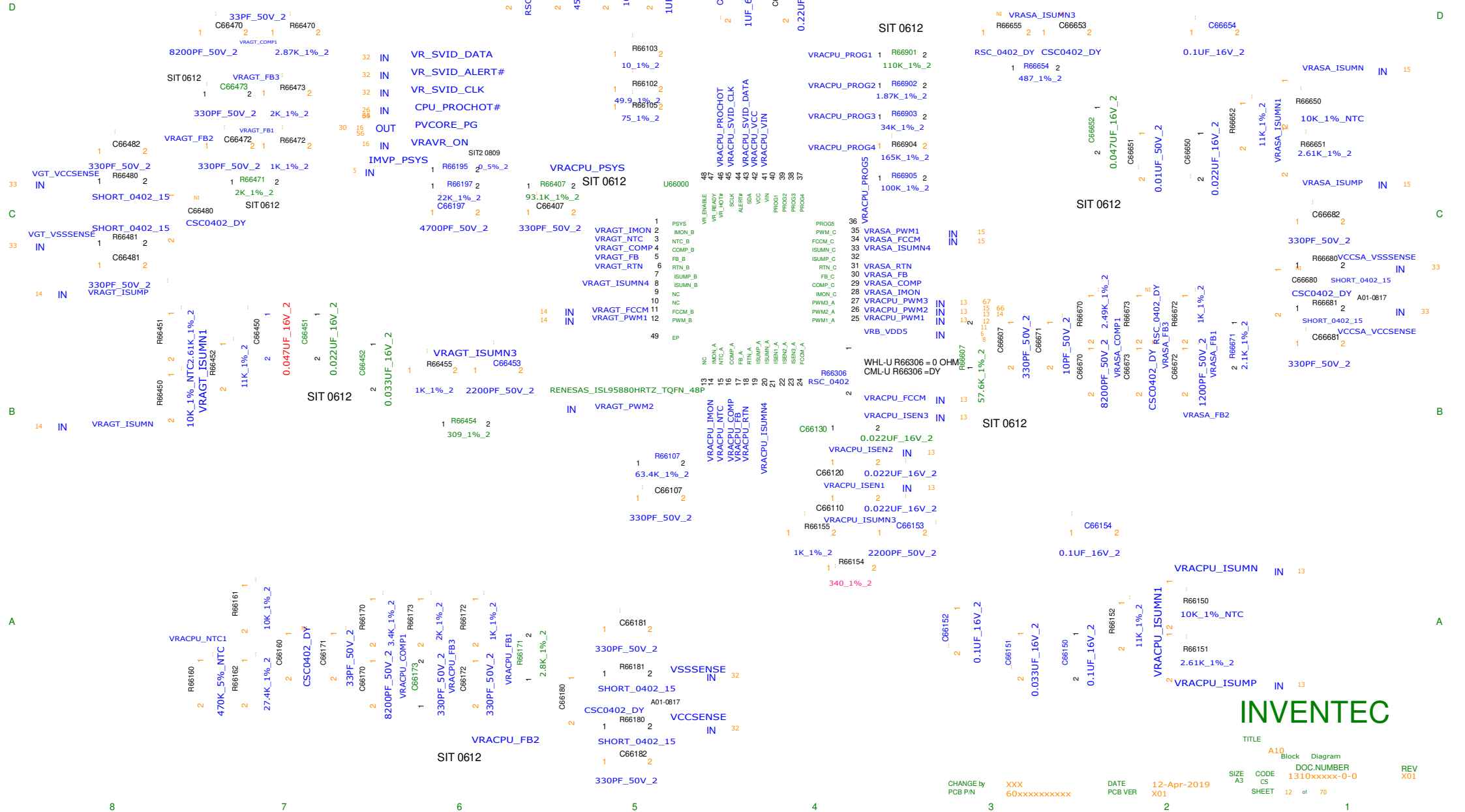


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A

REV
01

CONTROLLER



PVCORE

WS-0413

PVBAT_CPU_1

PVBAT

PVCORE

6014B0226601

PVBAT_CPU_1 OUT

SIT2 0725

PVBAT

PVBAT_CPU_2 OUT

PVBAT

PVBAT_CPU_3 OUT

SIT2 0730

C66003,6,7,8 BOM CHANGE TO OPEN

PVCORE

INVENTEC

TITLE
A10 Block Diagram
DOC NUMBER
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PCB P/N
XXX
60xxxxxxxxxx

DATE
PCB VER
12-Apr-2019
X01

REV
X01

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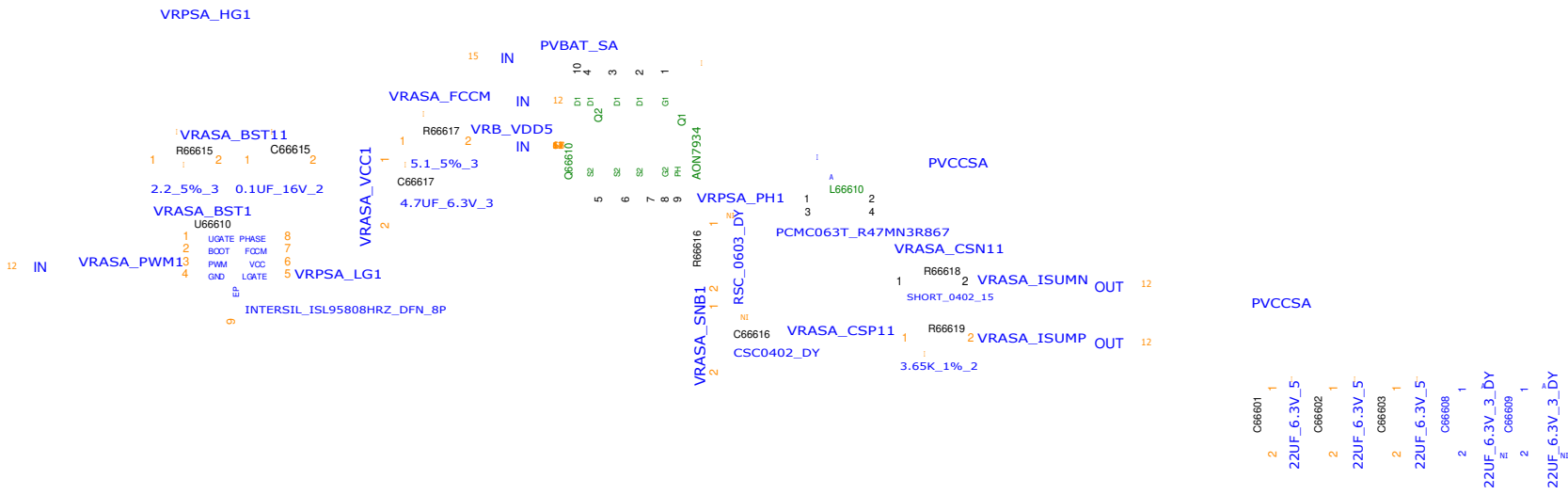
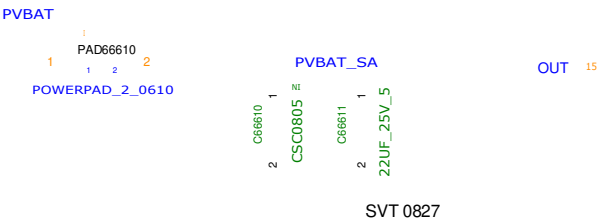
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3

2

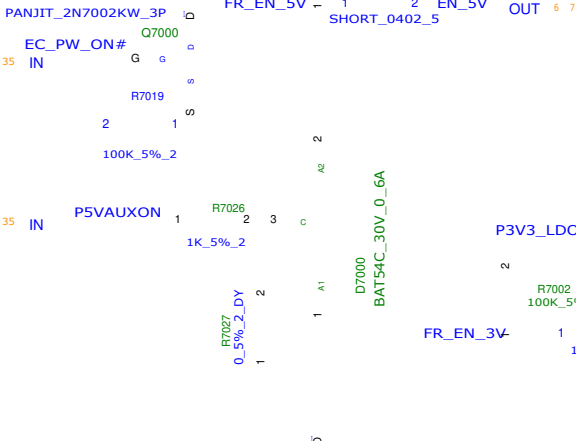
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PVCCSA

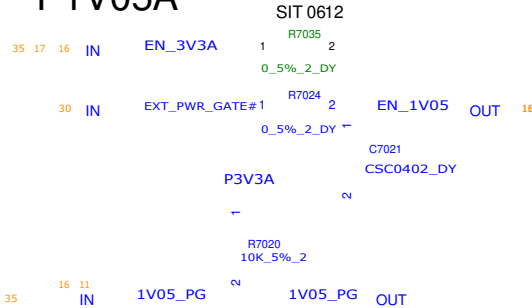


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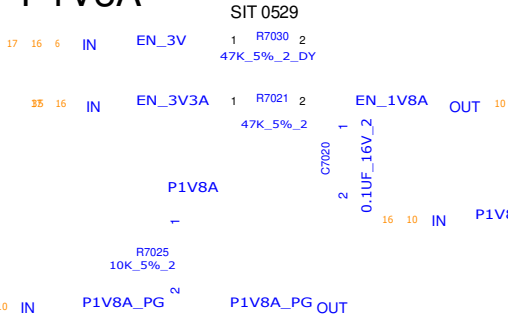
3V & 5V



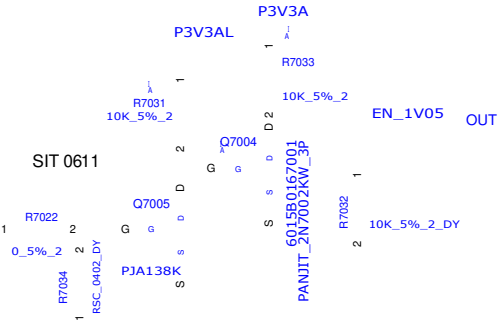
P1V05A



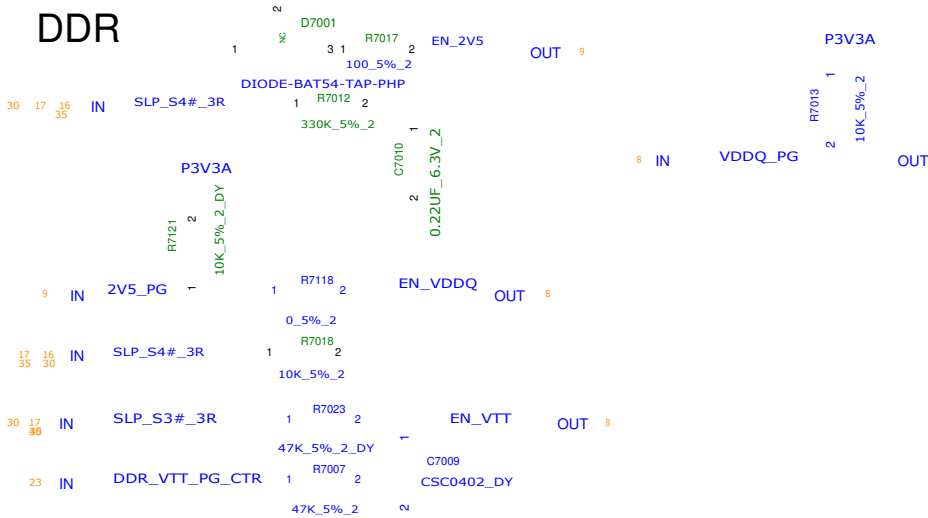
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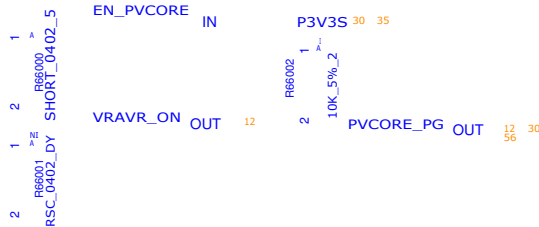
SIT 0611



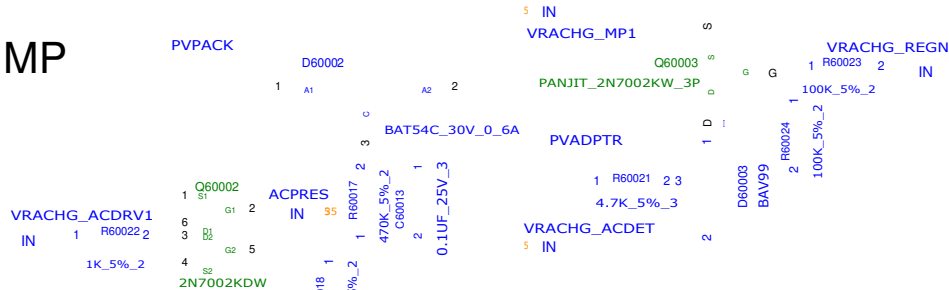
DDR



PVCORE



MP



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[illegible]

TITLE
A10 Block Diagram
SIZE CODE DOC.NUMBER REV
A3 CS 1310xxxxx-0-0 X01
SHEET 17 of 70

DATE 12-Apr-2019
PCB VER X01

REV
K01

REFERENCE 0~49(PCB SCREW)

D

C

B

A

FINGER1
1
EMI_STOP_SUL_15A3M_1P
FINGER2
1
EMI_STOP_SUL_15A3M_1P
FINGER3
1
EMI_STOP_SUL_15A3M_1P
FINGER4
1
EMI_STOP_SUL_15A3M_1P
FINGER5
1
EMI_STOP_SUL_15A3M_1P
FINGER6
1
EMI_STOP_SUL_15A3M_1P
FINGER7
1
EMI_STOP_SUL_15A3M_1P
FINGER8
1
EMI_STOP_SUL_15A3M_1P
FINGER9
1
EMI_STOP_SUL_15A3M_1P
FINGER10
1
EMI_STOP_SUL_15A3M_1P

FINGER11
1
EMI_STOP_SUL_15A3M_1P
FINGER12
1
EMI_STOP_SUL_15A3M_1P
FINGER13
1
EMI_STOP_SUL_15A3M_1P
FINGER14
1
EMI_STOP_SUL_15A3M_1P
FINGER15
1
EMI_STOP_SUL_15A3M_1P
FINGER16
1
EMI_STOP_SUL_15A3M_1P
FINGER17
1
EMI_STOP_SUL_15A3M_1P
FINGER18
1
EMI_STOP_SUL_15A3M_1P

FINGER40
1
EMI_STOP_QM_18G
FINGER41
1
EMI_STOP_QM_18G
FINGER42
1
EMI_STOP_QM_18G
FINGER43
1
EMI_STOP_QM_18G
FINGER44
1
EMI_STOP_QM_18G
FINGER45
1
EMI_STOP_QM_18G
FINGER46
1
EMI_STOP_QM_18G

CP22
1
EMI_STOP_SUL_15A8M_1P
CP23
1
EMI_STOP_SUL_15A8M_1P
CP24
1
EMI_STOP_SUL_15A8M_1P
CP29
1
EMI_STOP_SUL_15A8M_1P
CP30
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EMI_STOP_SUL_15A8M_1P
CP31
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EMI_STOP_SUL_15A8M_1P
CP32
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EMI_STOP_SUL_15A8M_1P

CP25
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EMI_STOP_SUL_15A8M_1P
CP26
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EMI_STOP_SUL_15A8M_1P
CP27
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EMI_STOP_SUL_15A8M_1P
CP28
1
EMI_STOP_SUL_15A8M_1P
CP33
1
EMI_STOP_SUL_15A8M_1P
CP34
1
EMI_STOP_SUL_15A8M_1P
CP35
1
EMI_STOP_SUL_15A8M_1P
CP36
1
EMI_STOP_SUL_15A8M_1P

D

C

B

A

GPU FAN
1 FIX1 1 FIX5 1 ST16 1 ST11
FIX_MASK FIX_MASK STDPAD_2.4_5.0_TOP STDPAD_3.15_5.5_TOP
1 FIX2 1 FIX6 1 ST17 1 ST12
FIX_MASK FIX_MASK STDPAD_2.4_5.0_TOP STDPAD_3.15_5.5_TOP
1 FIX3 1 FIX7 1 ST13
FIX_MASK FIX_MASK STDPAD_3.15_5.5_TOP
1 FIX4 1 FIX8 1 ST18
FIX_MASK FIX_MASK STDPAD_3.15_5.5_TOP

ST14
STANDOFF_3.2_6.0
2.33MM
ST15 SSD
STDPAD_320_750_600_1P
1.25MM

CPU

ST1
STDPAD_2.4_5.0_TOP
0.9MM
ST2
STDPAD_2.4_5.0_TOP
0.9MM
ST3
STDPAD_2.4_5.0_TOP
0.9MM
ST4
STDPAD_2.4_5.0_TOP
0.9MM

PCB

S2
SCREW230_500_1P
S3
SCREW230_500_1P
S4
SCREW230_500_1P
S5
SCREW230_500_1P
S6
SCREW230_500_1P
S7
SCREW230_500_1P
S9
SCREW230_500_1P

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TITLE
A10 Block Diagram
DOC.NUMBER
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REV
X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 12-Apr-2019
PCB VER X01

SIZE A3
CODE CS
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A



DDR4

F

F

E

E

D

D

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B

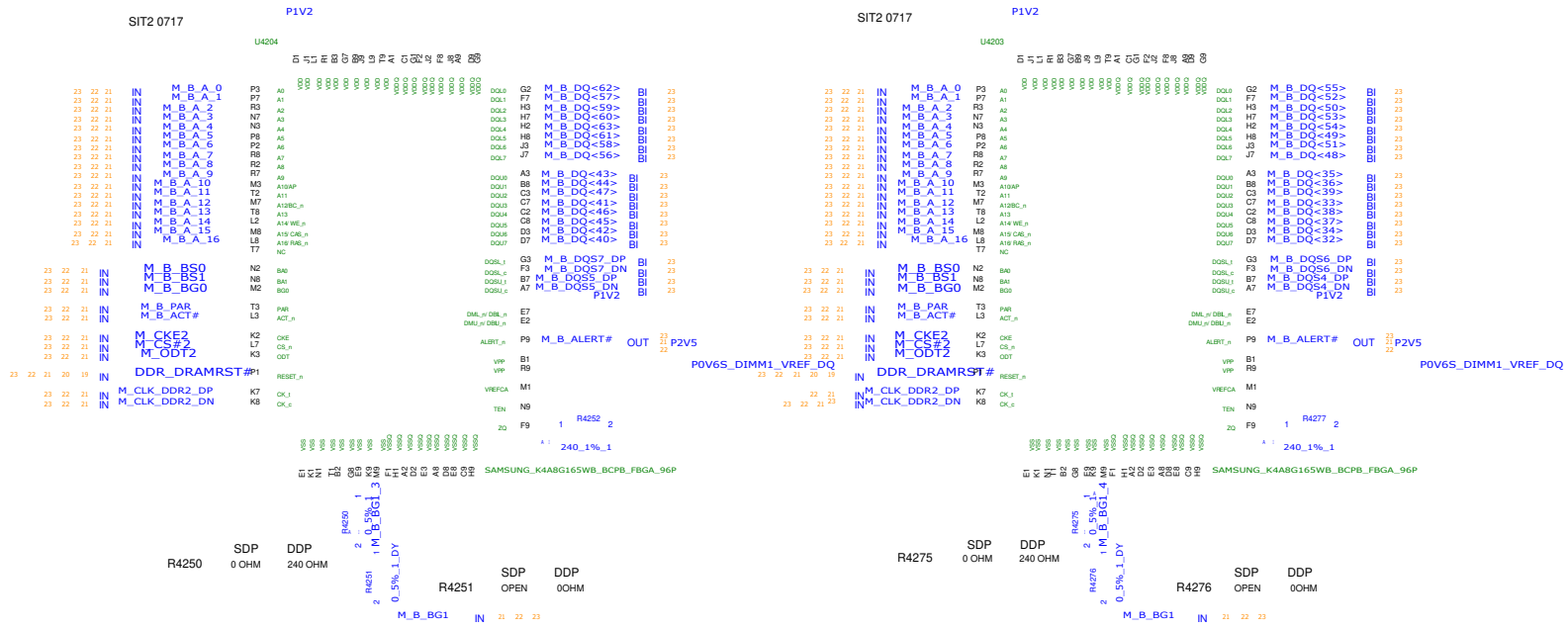
A

A

REFERENCE NUMBER:4100~4299

INVENTEC

DDR4



REFERENCE NUMBER:4100~4299

INVENTEC

REFERENCE:4500~4949

F

E

D

C

A

U4500

A26
D26
D28
C28
B26
B28
B30
A28
D30
B32
D32
A30
C30
B32
C32
H34
H36
H38
H35
K36
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A500

V32 M_CLK_DDR0_DN OUT 19 20
V31 M_CLK_DDR0_DP OUT 19 20
T32 M_CLK_DDR1_DN OUT 19 20
T31 M_CLK_DDR1_DP OUT 19 20
U36 M_CKE0 OUT 19 20
U37 M_CKE1 OUT 19 20
U38 M_CKE2 OUT 19 20
U39 M_CKE3 OUT 19 20
AE32 M_CS#0 OUT 19 20
AF32 M_CS#1 OUT 19 20
AE31 M_ODT0 OUT 19 20
AF31 M_ODT1 OUT 19 20
AC37 M_A_A_0 OUT 19 20
AC38 M_A_A_1 OUT 19 20
AC39 M_A_A_2 OUT 19 20
AC35 M_A_A_3 OUT 19 20
AA35 M_A_A_4 OUT 19 20
AA36 M_A_A_5 OUT 19 20
AA37 M_A_A_6 OUT 19 20
AA38 M_A_A_7 OUT 19 20
AA39 M_A_A_8 OUT 19 20
W36 M_A_A_9 OUT 19 20
V31 M_A_A_10 OUT 19 20
W34 M_A_A_11 OUT 19 20
AA38 M_A_A_12 OUT 19 20
AC32 M_A_A_13 OUT 19 20
AC31 M_A_A_14 OUT 19 20
AA32 M_A_A_15 OUT 19 20
Y32 M_A_A_16 OUT 19 20
W32 M_A_B0 OUT 19 20
AE31 M_A_B01 OUT 19 20
V34 M_A_B02 OUT 19 20
V35 M_A_ACT# OUT 19 20
W35 M_A_B01 OUT 19 20
C27 M_A_DQ0_DN BI 19
C27 M_A_DQ0_DP BI 19
C31 M_A_DQ1_DN BI 19
C31 M_A_DQ1_DP BI 19
C35 M_A_DQ2_DN BI 20
C35 M_A_DQ2_DP BI 20
P34 M_A_DQ3_DN BI 20
P34 M_A_DQ3_DP BI 20
P35 M_A_DQ4_DN BI 20
P35 M_A_DQ4_DP BI 20
AP35 M_B_DQ0_DN BI 21
AP35 M_B_DQ0_DP BI 21
AV35 M_B_DQ1_DN BI 21
AV35 M_B_DQ1_DP BI 21
BB35 M_B_DQ2_DN BI 21
BB35 M_B_DQ2_DP BI 21
BF34 M_B_DQ3_DN BI 22
BF34 M_B_DQ3_DP BI 22
BF35 M_B_DQ4_DN BI 22
BF35 M_B_DQ4_DP BI 22
W37 M_A_ALERT# IN 19 20
W31 M_A_PAR IN 19 20
F36 DQS OUT 19 20
D35 1 T4515 OUT 19 20
D37 OUT 19 20
E36 OUT 19 20
C36 DDR_VTT_CTRL OUT 23

POV6M_VREF_H

POV6M_VREF_DQ

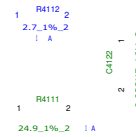
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POV6S_DIMM1_VREF_DQ

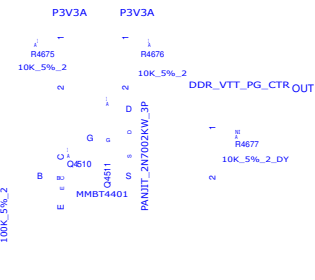
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POV6M_VREF_H



INTEL_J86075_BGA_1528P



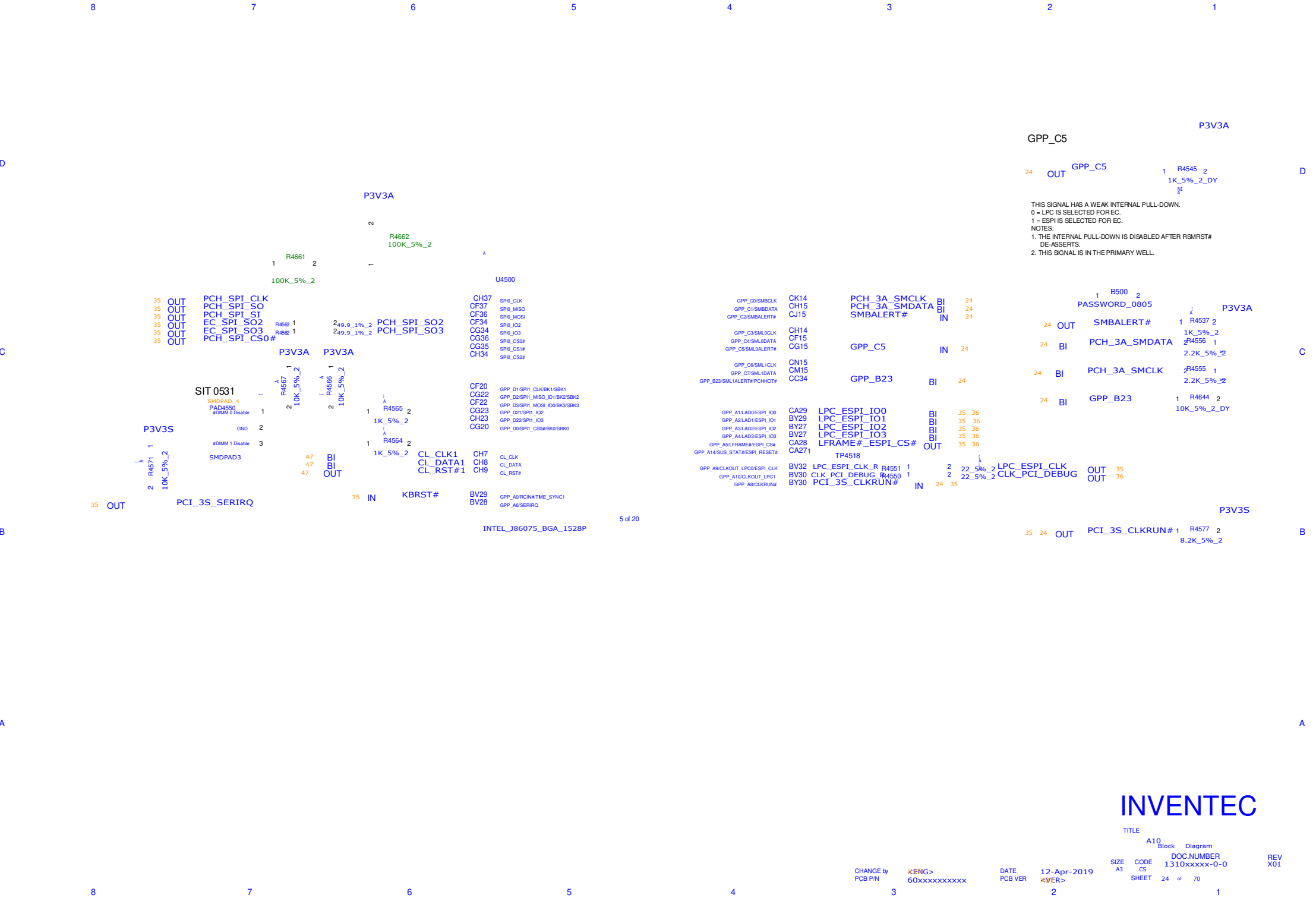
DDR_VTT_PG_CTRL OUT 16

DDR_DRAMRST#_CPU OUT 23

DDR_DRAMRST# IN 19 20 21 22

0.1UF_6.3V_1_DY

INVENTEC



REFERENCE 4700~4949(PCH)

P3V3A

```
1 R4595 2 GPU_EVENT_PCH# OUT 25 64
10K_5%_2
```

P3V3S

GPP_B22

P3V3A

2 R4904 1 GPP_B22 OUT 25
10K_5%_2_DY
BOOT BIOS STRAP BIT
0 SPI (DEFAULT)
1 LPC

P3V3A

GPP_B18

GPP_B18: R4596

0 = DISABLE NO REBOOT MODE(DEFAULT)
1 = ENABLE NO REBOOT MODE

U4500

INTEGRATED SENSOR HUB

3

1V8

3V3

GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#

P3V3A

I2C0 USE FOR TOUCHPAD

1	R4558	2	PCH_I2C_DATA	BI	25	37
1	2.2K_5%_2					
1	R4557	2	PCH_I2C_CLK	BI	25	37
1	2.2K_5%_2					

1	R4561	2	PCH_I2C1_DATA	BI	25	52
2.2K_5%-2_DY						
1	R4560	2	PCH_I2C1_CLK	BI	25	52
2.2K_5%-2_DY						

P1V8A

1	R4909	2	10K_5%_2_DY	CNV_BRI_RSP	BI	25	47
1	R4913	2	10K_5%_2_DY	CNV_RGI_RSP	BI	25	47

PLACEMENT CLOSE TO PCH

P1V8A

R4950	1	2	20K_5%_2_DY	CNV_BRI_DT_R	BI	35
R4951	1	2	20K_5%_2	CNV_RGI_DT_R	BI	25 47

PLACEMENT CLOSE TO WLAN(U1300)

CA31	GPP_B19/GSP1_CS0#
CA32	GPP_A11/PME#/GSP1_CS1#SD_VDD2_PWR_EN#
HCC29	GPP_B20/GSP1_CLK
CC30	GPP_B21/GSP1_MISO
CA30	GPP_B22/GSP1_MOSI
CK20	STRAP
CG19	GPP_F5/CNV_BRI_RSP
CJ20	GPP_F6/CNV_RGI_DT
CH19	GPP_F4/CNV_BRI_DT
	GPP_F7/CNV_RGI_RSP

CR12	GPP_C20/UART2_RXD
CP12	GPP_C21/UART2_TXD
CN12	GPP_C22/UART2_RTS#
CM12	GPP_C23/UART2_CTS#
CM11	GPP_C16/I2C0_SDA
CN11	GPP_C17/I2C0_SCL
CK12	GPP_C18/I2C1_SDA
CJ12	GPP_C19/I2C1_SCL

CF27	GPP_H4/12C2_SDA
CF29	GPP_H5/12C2_SCL
CH27	GPP_H6/12C3_SDA
CH28	GPP_H7/12C3_SCL
CJ30	GPP_H8/12C4_SDA
CJ31	GPP_H9/12C4_SCL

INTEL_J86075_BGA_1528P

CNV_RGI_DT_R OUT 25 47

CNV STRAP
1= CNVIDISABLE
0= CNVIEABLE

CNVI_RGI_DT_PIN GETS THE PULL-DOWN RESISTOR (1K OHM) FROM THE INTERNAL CRF MODULE WHEN CNVI IS ENABLED. THERE MUST NOT BE ANY PULL-DOWN RESISTOR CONNECTED ON THE BOARD.

INVENTEC

```

TITLE
A10
Block Diagram
DOC.NUMBER
SIZE CODE 1310xxxxx-0-0

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REV
K01

D

D

C

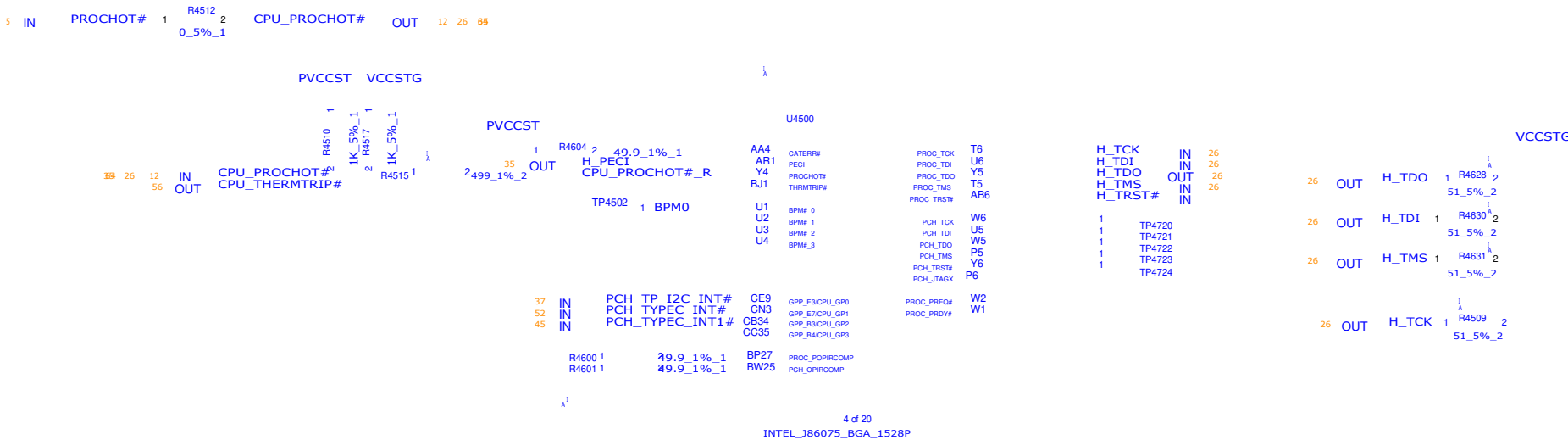
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B

B

A

A



DGPU PRSNT#

DGPU_PRSNT#

DIS 0

UMA 1

INVENTEC

TITLE

A10 Block Diagram

DOC.NUMBER 1310xxxx-0-0

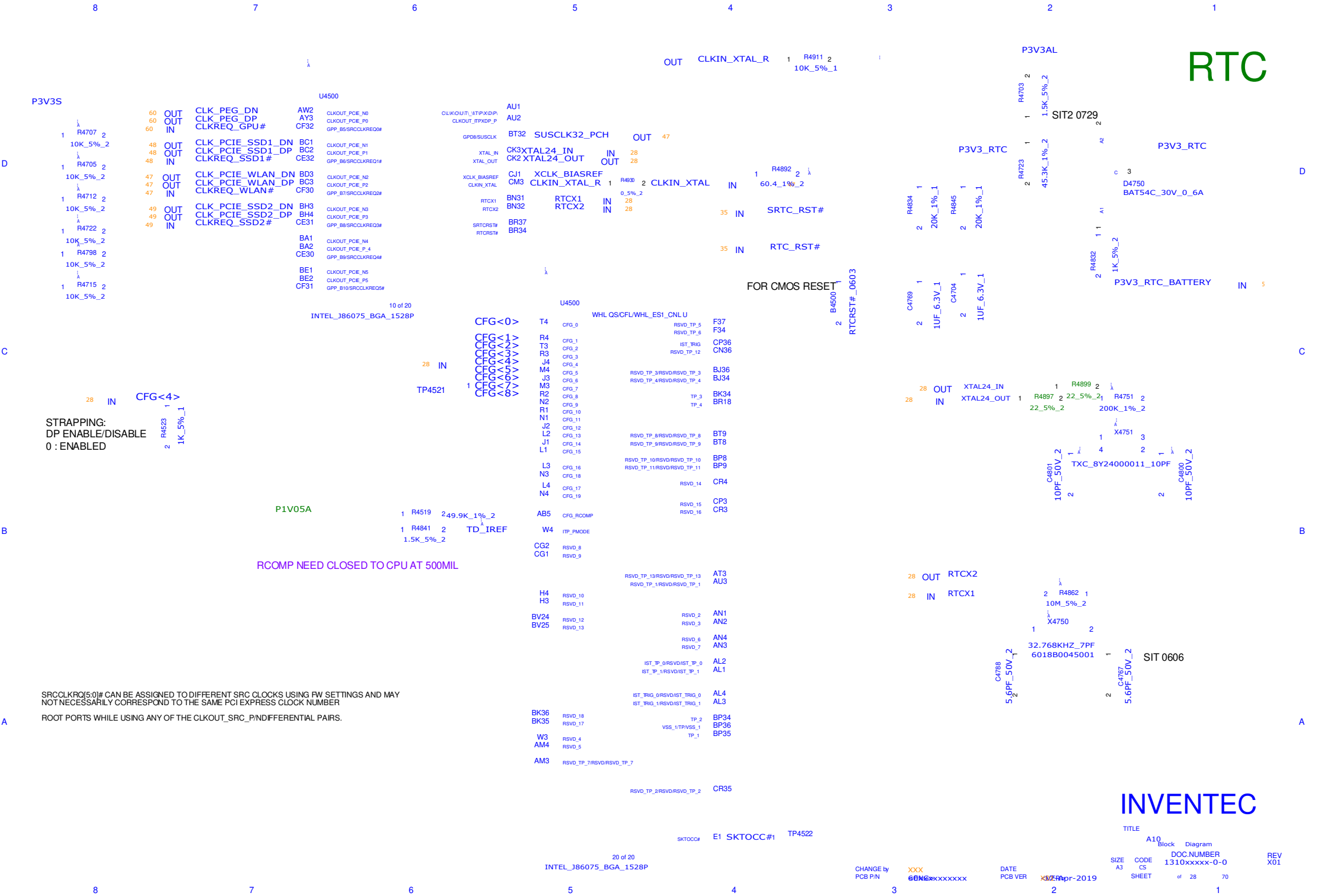
REV X01

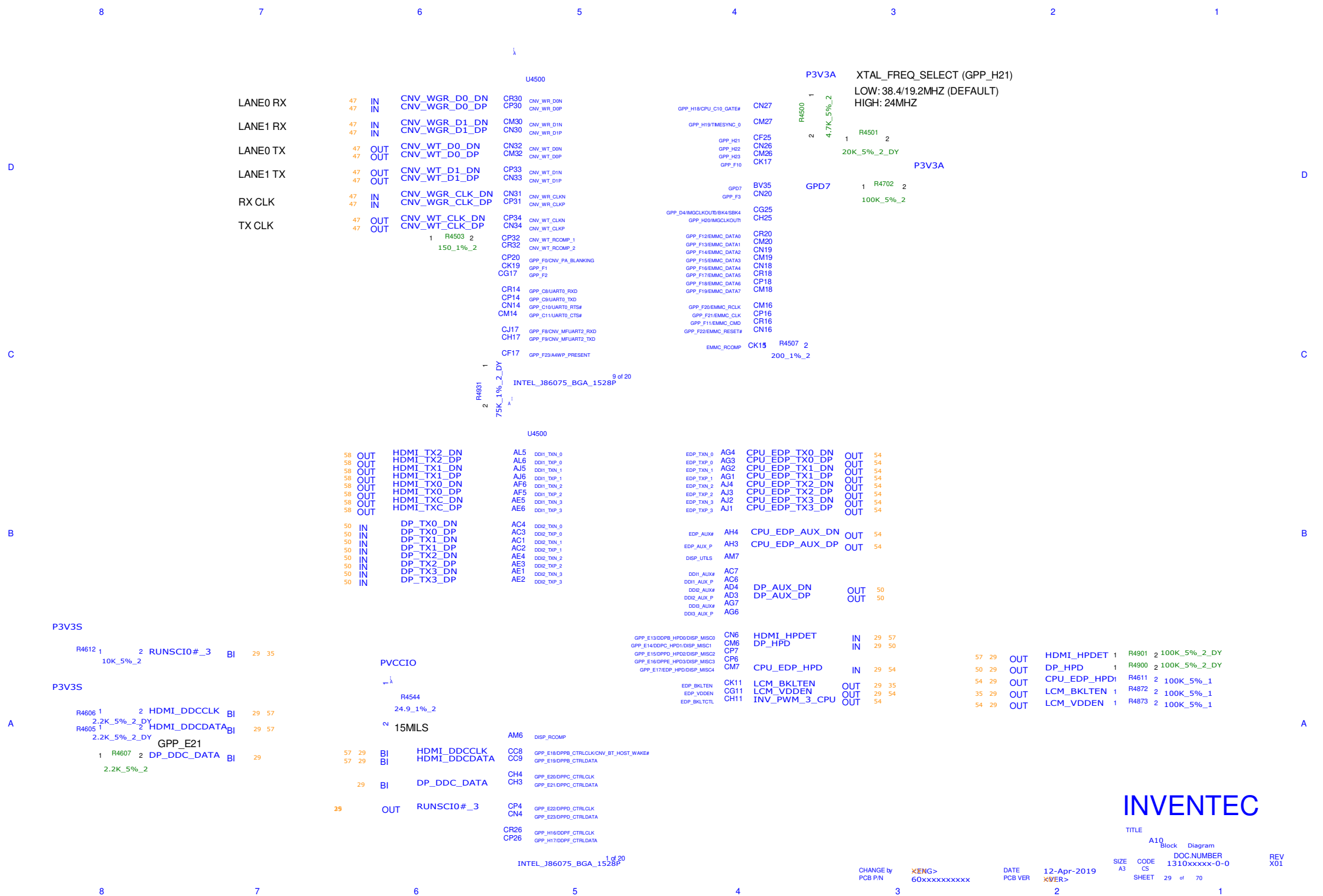
CHANGE by XENG> 60xxxxxxxxxx

DATE PCB VER 12-Apr-2019 XVER>

SIZE A3 CODE CS SHEET 26 of 70









TITLE
A10 Block Diagram
SIZE CODE DOC.NUMBER
A3 CS 1310xxxxx-0-0
SHEET 30 of 70

DATE 12-Apr-2019
PCB VER ~~XIV~~ER>

U4500			
CR34	VSS_342	VSS_330	BL7
BT5	VSS_351	VSS_337	AE25
BY5	VSS_361	VSS_345	BM33
CP35	VSS_371	VSS_354	CM5
CM37	VSS_381	VSS_364	AE27
CK37	VSS_391	VSS_374	BM35
AW1	VSS_401	VSS_384	CM9
CM1	VSS_411	VSS_392	AE30
BD6	VSS_421	VSS_398	BM36
AY4	VSS_360	VSS_315	CN13
B34	VSS_370	VSS_322	AE7
E35	VSS_380	VSS_329	BM9
A4	VSS_390	VSS_336	CN17
AE24	VSS_400	VSS_344	AF27
AE26	VSS_410	VSS_353	BN30
AF25	VSS_420	VSS_363	CN21
AG24	VSS_428	VSS_373	AF3
AG26	VSS_434	VSS_395	BN7
AH24	VSS_396	VSS_301	CN25
AH25	VSS_350	VSS_307	AF30
B2	VSS_359	VSS_314	CN29
B36	VSS_369	VSS_321	AF33
C36	VSS_379	VSS_328	BP15
C37	VSS_389	VSS_335	AF36
CN1	VSS_399	VSS_343	AF4
CN2	VSS_409	VSS_352	CN5
CN37	VSS_419	VSS_362	AF7
CP2	VSS_427	VSS_416	BP25
D1	VSS_433	VSS_425	CN9
A32	VSS_341	VSS_432	AG10
F33	VSS_349	VSS_294	BP3
A3	VSS_358	VSS_300	CP1
BJ7	VSS_368	VSS_306	BP32
CJ36	VSS_378	VSS_313	CP11
A36	VSS_388	VSS_320	AN7
BK10	VSS_398	VSS_327	BP33
CJ4	VSS_408	VSS_334	CP13
AB27	VSS_418	VSS_405	AH28
BK2	VSS_426	VSS_415	BP4
CK1	VSS_333	VSS_424	CP15
AB3	VSS_340	VSS_431	AH29
BK28	VSS_348	VSS_293	BP7
AB30	VSS_357	VSS_299	CP19
BK3	VSS_367	VSS_305	AH30
CK4	VSS_377	VSS_312	CP21
AB33	VSS_387	VSS_319	AH31
BK33	VSS_397	VSS_326	BR19
CK7	VSS_407	VSS_334	CP27
AB36	VSS_417	VSS_404	AH33
BK4	VSS_325	VSS_414	BR25
CL2	VSS_332	VSS_423	AH35
AB4	VSS_339	VSS_430	CP37
BK7	VSS_347	VSS_292	AJ25
CM13	VSS_356	VSS_298	BT15
AB7	VSS_366	VSS_304	AJ28
BL25	VSS_376	VSS_311	BT16
CM17	VSS_386	VSS_318	CP9
AC10	VSS_396	VSS_383	AJ7
BL28	VSS_406	VSS_393	CR2
CM21	VSS_317	VSS_403	AK3
AC27	VSS_413	VSS_413	CR36
BL29	VSS_331	VSS_422	AK33
CM25	VSS_338	VSS_429	D21
AC30	VSS_346	VSS_291	AK36
BL30	VSS_355	VSS_297	D25
CM29	VSS_365	VSS_303	AK4
BL31	VSS_375	VSS_310	BT28
CM31	VSS_385	VSS_372	AL28
AD33	VSS_395	VSS_382	BT33
BL32	VSS_399	VSS_392	D5
CM33	VSS_316	VSS_402	AL29
AD35	VSS_323	VSS_412	

17 of 20
INTEL_J86075_BGA_1528P

U4500			
BT35	VSS_277	VSS_180	BY25
D6	VSS_290	VSS_183	J18
AL32	VSS_156	VSS_186	AU32
BT36	VSS_165	VSS_245	BY28
D8	VSS_172	VSS_257	J21
AL7	VSS_208	VSS_270	BY33
D9	VSS_217	VSS_284	J24
AM10	VSS_227	VSS_151	AV28
BU11	VSS_238	VSS_161	BY35
E23	VSS_250	VSS_169	J33
AM28	VSS_263	VSS_175	AV3
E27	VSS_276	VSS_179	BY36
AM33	VSS_289	VSS_182	J36
BU23	VSS_155	VSS_233	AV33
E29	VSS_164	VSS_244	J6
AM35	VSS_200	VSS_256	AV36
BU24	VSS_207	VSS_269	C1
E31	VSS_216	VSS_283	K21
BU25	VSS_226	VSS_150	AV4
E33	VSS_237	VSS_160	C21
AN25	VSS_249	VSS_168	K22
BU7	VSS_262	VSS_174	AV6
E9	VSS_275	VSS_178	C25
AN28	VSS_288	VSS_222	K24
BV11	VSS_154	VSS_232	AV8
F12	VSS_194	VSS_243	C29
AN29	VSS_199	VSS_255	K25
F15	VSS_208	VSS_268	AW28
AN30	VSS_215	VSS_282	C33
F18	VSS_225	VSS_149	K27
AN31	VSS_236	VSS_159	AW29
BV3	VSS_248	VSS_167	C4
F2	VSS_261	VSS_173	K29
AN7	VSS_274	VSS_212	AW3
BV31	VSS_287	VSS_221	C9
F21	VSS_189	VSS_231	K29
AN8	VSS_193	VSS_242	CA11
BV33	VSS_198	VSS_254	AW30
F24	VSS_205	VSS_267	K3
BV4	VSS_214	VSS_281	AW31
F3	VSS_224	VSS_148	CA15
AP3	VSS_235	VSS_158	K30
BW11	VSS_247	VSS_166	AY33
F4	VSS_260	VSS_203	CA22
AP33	VSS_273	VSS_211	K31
BW15	VSS_185	VSS_220	AY35
G21	VSS_188	VSS_230	K32
AP36	VSS_197	VSS_253	B12
G27	VSS_197	VSS_253	K4
AP4	VSS_204	VSS_266	B15
G33	VSS_213	VSS_280	CA25
AR28	VSS_223	VSS_147	U7
G35	VSS_234	VSS_157	B18
G36	VSS_246	VSS_196	CB11
AT33	VSS_259	VSS_202	L27
BW24	VSS_272	VSS_210	B21
G9	VSS_286	VSS_219	L33
AT35	VSS_153	VSS_229	B23
H21	VSS_163	VSS_240	L35
AT36	VSS_171	VSS_252	B25
BW7	VSS_177	VSS_265	CB18
H27	VSS_181	VSS_279	L36
AT4	VSS_184	VSS_146	B27
BY11	VSS_187	VSS_190	CB19
AU10	VSS_191	VSS_195	L6
BY15	VSS_258	VSS_201	B29
H9	VSS_271	VSS_209	CB2
AU28	VSS_285	VSS_218	N25
BY22	VSS_152	VSS_228	B31
J12	VSS_162	VSS_239	CB20
AU29	VSS_170	VSS_251	N27
J15	VSS_176	VSS_264	CB25
		VSS_278	

18 of 20
INTEL_J86075_BGA_1528P

U4500			
N6	VSS_66	VSS_99	CF23
B37	VSS_73	VSS_106	V4
CB3	VSS_79	VSS_115	BE30
P10	VSS_84	VSS_126	CF28
B5	VSS_89	VSS_139	W10
CB33	VSS_95	VSS_8	BE31
P3	VSS_102	VSS_19	CF3
B7	VSS_110	VSS_29	W27
CB4	VSS_120	VSS_33	CF4
P33	VSS_132	VSS_87	W30
B9	VSS_145	VSS_92	BF3
CB7	VSS_14	VSS_98	CG33
P36	VSS_25	VSS_105	W7
BA10	VSS_35	VSS_114	BF33
CC11	VSS_44	VSS_125	CG7
P4	VSS_52	VSS_138	BF36
BA28	VSS_59	VSS_7	Y26
P7	VSS_65	VSS_18	BF4
BA3	VSS_72	VSS_77	CH31
CC20	VSS_78	VSS_82	Y27
R27	VSS_86	VSS_131	BG25
BB3	VSS_144	VSS_91	Y30
CC25	VSS_13	VSS_97	BG28
R28	VSS_24	VSS_104	CJ11
BB33	VSS_34	VSS_113	Y33
CC28	VSS_43	VSS_124	CJ14
R29	VSS_51	VSS_137	Y35
BB36	VSS_58	VSS_6	BH28
CC31	VSS_64	VSS_70	CJ19
R30	VSS_71	VSS_76	Y7
BB4	VSS_119	VSS_81	BH29
CC7	VSS_130	VSS_85	CJ23
R31	VSS_143	VSS_90	BH32
BC25	VSS_12	VSS_96	CJ28
CD11	VSS_23	VSS_103	BH33
T27	VSS_33	VSS_112	CJ33
CD12	VSS_42	VSS_123	BH35
T30	VSS_50	VSS_136	CJ35
BC29	VSS_57	VSS_139	BP19
CD14	VSS_63	VSS_17	BR16
T33	VSS_109	VSS_28	BY18
T35	VSS_118	VSS_38	BY19
BC32	VSS_129	VSS_47	CC16
CD24	VSS_142	VSS_55	BU16
T36	VSS_11	VSS_62	CC14
CD25	VSS_22	VSS_69	BR22
T7	VSS_32	VSS_75	BU20
BC8	VSS_41	VSS_81	CD20
CE33	VSS_49	VSS_135	BT14
U26	VSS_56	VSS_4	BP12
BD28	VSS_101	VSS_16	CB24
CE35	VSS_108	VSS_27	CC24
J5	VSS_117	VSS_37	U24
BD33	VSS_128	VSS_46	BD7
CE36	VSS_141	VSS_54	AR4
V26	VSS_10	VSS_61	AU4
BD35	VSS_21	VSS_68	AW4
CE7	VSS_31	VSS_74	BA6
V27	VSS_40	VSS_122	BC4
BD36	VSS_48	VSS_134	BE4
CF11	VSS_53	VSS_94	BE8
V3	VSS_100	VSS_15	BA4
BE10	VSS_107	VSS_26	BD4
CF14	VSS_116	VSS_36	BG4
V30	VSS_127	VSS_45	CJ2
BE28	VSS_140	VSS_53	CJ3
CF19	VSS_60	VSS_9	AM5
V33	VSS_20	VSS_67	CM4
BE29	VSS_30	VSS_111	AC5
CF2	VSS_39	VSS_121	AG5
V36	VSS_88	VSS_133	CR6
BE3	VSS_93	VSS_2	

19 of 20
INTEL_J86075_BGA_1528P

INVENTEC

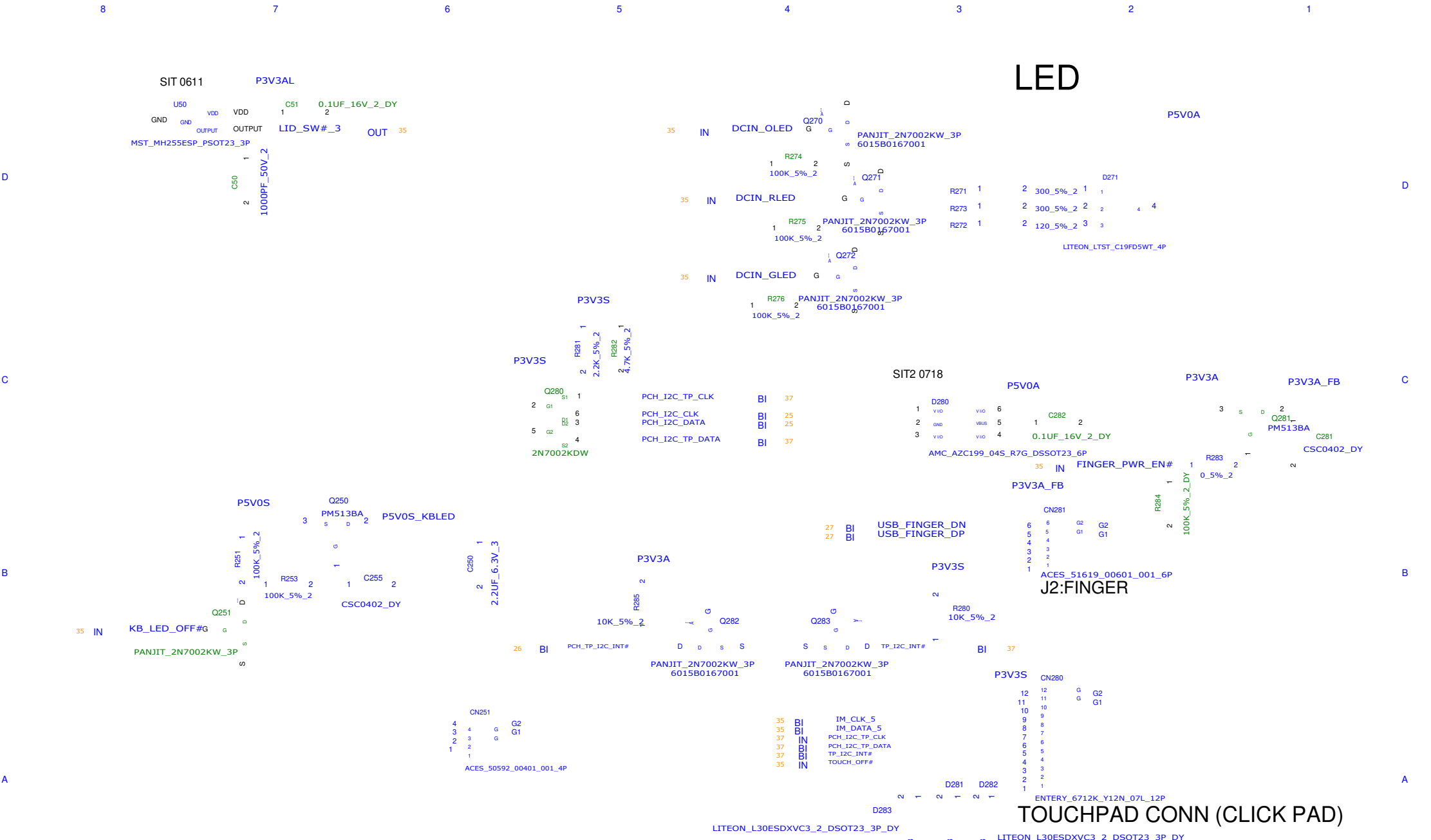
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DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET 34 of 70

CHANGE by
PCB P/N
XENG>
60xxxxxxxxxx

DATE
PCB VER
12-Apr-2019
XVER>

[illegible]

LED



KEYBOARD LED CONN

TOUCHPAD CONN (CLICK PAD)

INVENTEC

TITLE		A10		Block		Diagram		DOC NUMBER		REV	
SIZE	A3	CODE	CS	SHEET	37	of	70	1310xxxxx-0-0		X01	
CHANGE by	PCB P/N	XXX	60xxxxxxxxxxx	DATE	PCB VER	12-Apr-2019	X01				

TIED UNDER OR NEAR CODEC



CHANGE by PCB P/N	ENG 60xxxxxxxxxx	DATE PCB VER	12-Apr-2019 VER
3			2

AUDIO JACKS

MIC2_VREFO IN 38 39

2
R600
2.2K_5%_2
1

39 BI MIC
1 R611 2
SHORT_0402_15
CSC0402_DY
2 C605

SLEEVE BI 38

EMI CAPACITORS TO CLOSE TO JACK SIDE

AGND_AUDIO

MIC2_VREFO IN 38 39

2
R601
2.2K_5%_2
1

39 BI RING2_CONN
1 R612 2
SHORT_0402_15
CSC0402_DY
2 C604

RING2 BI 38

EMI CAPACITORS TO CLOSE TO JACK SIDE

AGND_AUDIO

38 IN LINE1_VREFO_L 1 R607 2 4.7K_5%_2_DY
38 IN LINE1_VREFO_R 1 R606 2 4.7K_5%_2_DY

38 IN LINE1_L 1 C602 2
4.7UF_6.3V_3_DY
38 IN HP_L
38 IN HP_R

38 IN LINE1_R 1 C603 2
4.7UF_6.3V_3_DY

SVT 0917

D600
LITEON_L30ESDXVC3_2_DSOT23_3P
3 2
1

1 R605 2
22_5%_2
1 R604 2
22_5%_2

39 BI RING2_CONN
38 OUT HPS
39 BI MIC

JACK601
3 GM 1 L
5 5
6 6
2 2 R
4 4 MG
MS MS

SINGA_2SJ3095_166111F_6P

AGND_AUDIO

SVT 0917

RESERVE FOR EMI

AGND_AUDIO

2 C601 1
470PF_50V_2
2 C600 1
470PF_50V_2
D601 2
1 SFT_SF10402ML120C_LF_SMD_2P
D602 1
2 SFT_SF10402ML120C_LF_SMD_2P
D603 1
2 SFT_SF10402ML120C_LF_SMD_2P

INVENTEC

TITLE
A10 Block Diagram
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET
39 of 70

CHANGE by XXXX
PCB P/N 60xxxxxxxxxx
DATE 12-Apr-2019
PCB VER X01

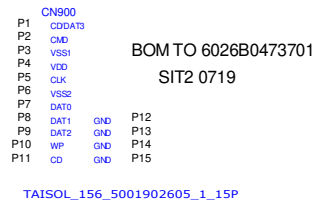
F

E

2

A

CARD READER



REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1

D

D

C

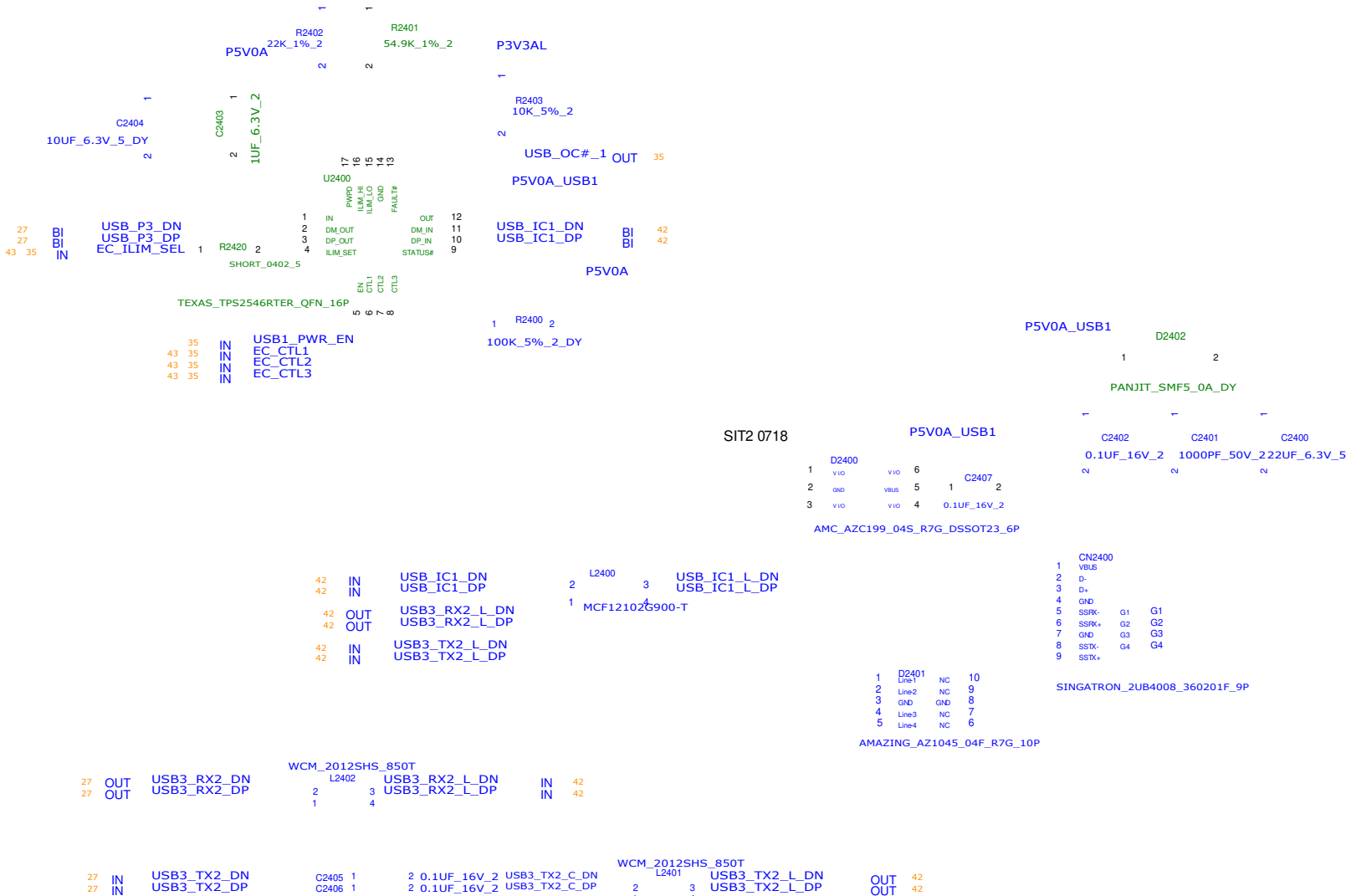
C

B

B

A

A



INVENTEC

CHANGE by
PCB P/N XXXX
60xxxxxxxxxx

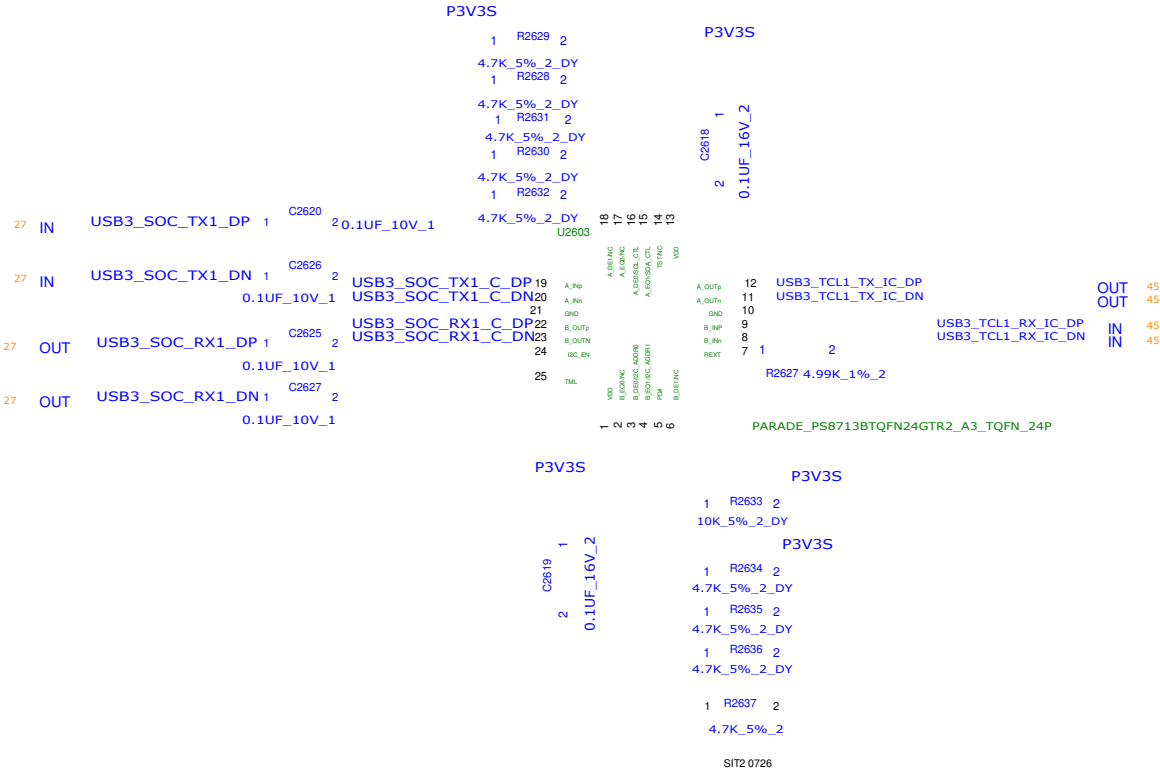
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X01

TITLE
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DOC NUMBER
1310xxxx-0-0
SHEET 42 of 70

REV
X01

USB3 REDRIVER 1

REFERENCE 2600~2699(USB RESERVE)



INVENTEC

TITLE
A10 Block Diagram
DOC NUMBER
1310xxxx-0-0
REV
X01

CHANGE by
PCB P/N XXX
60xxxxxxxxxx

DATE
PCB VER 12-Apr-2019
X01

SIZE
A3
CODE
CS
SHEET 44 of 70

REV
X01

A

EV
01

A B C D E F

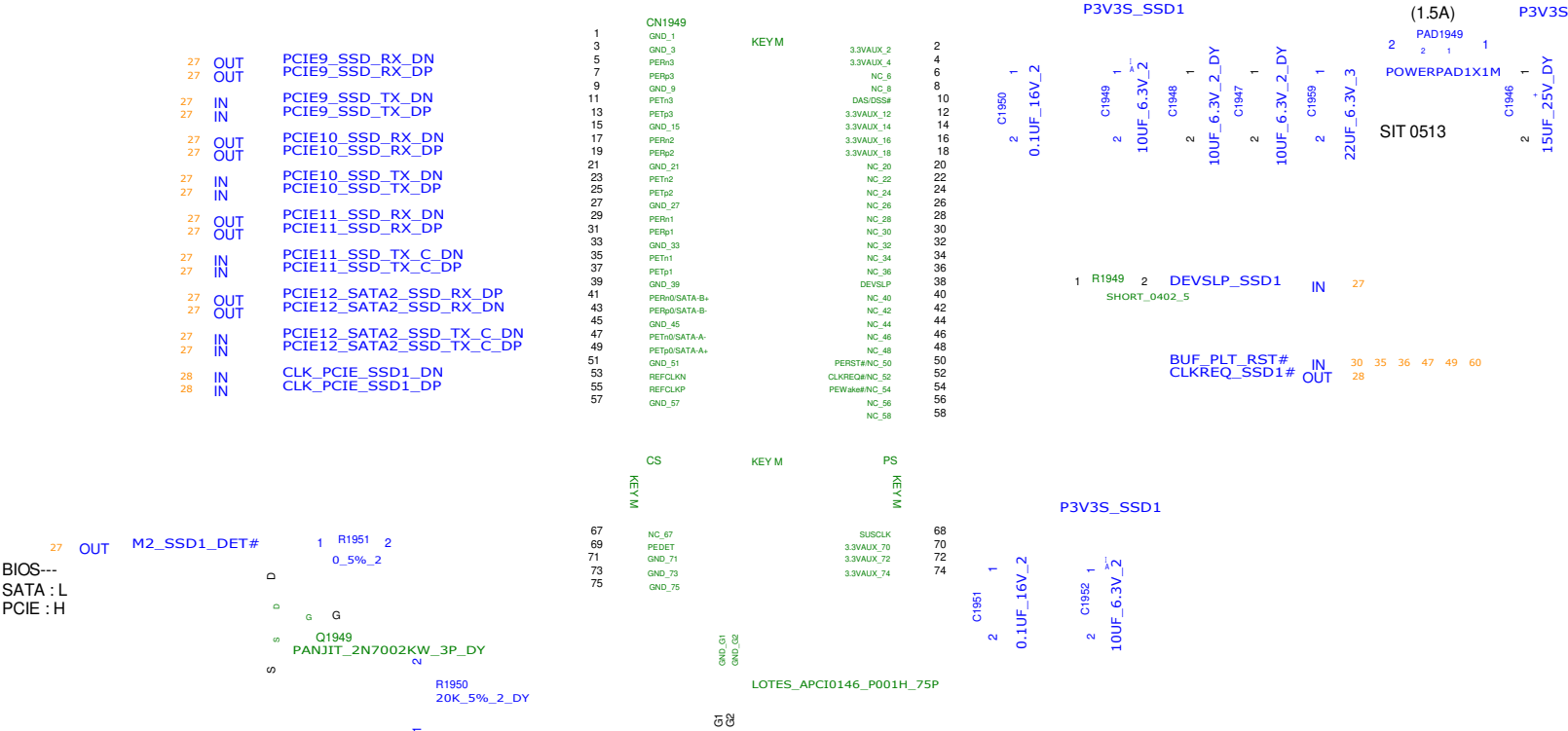


REFERENCE 1300 ~ 1349



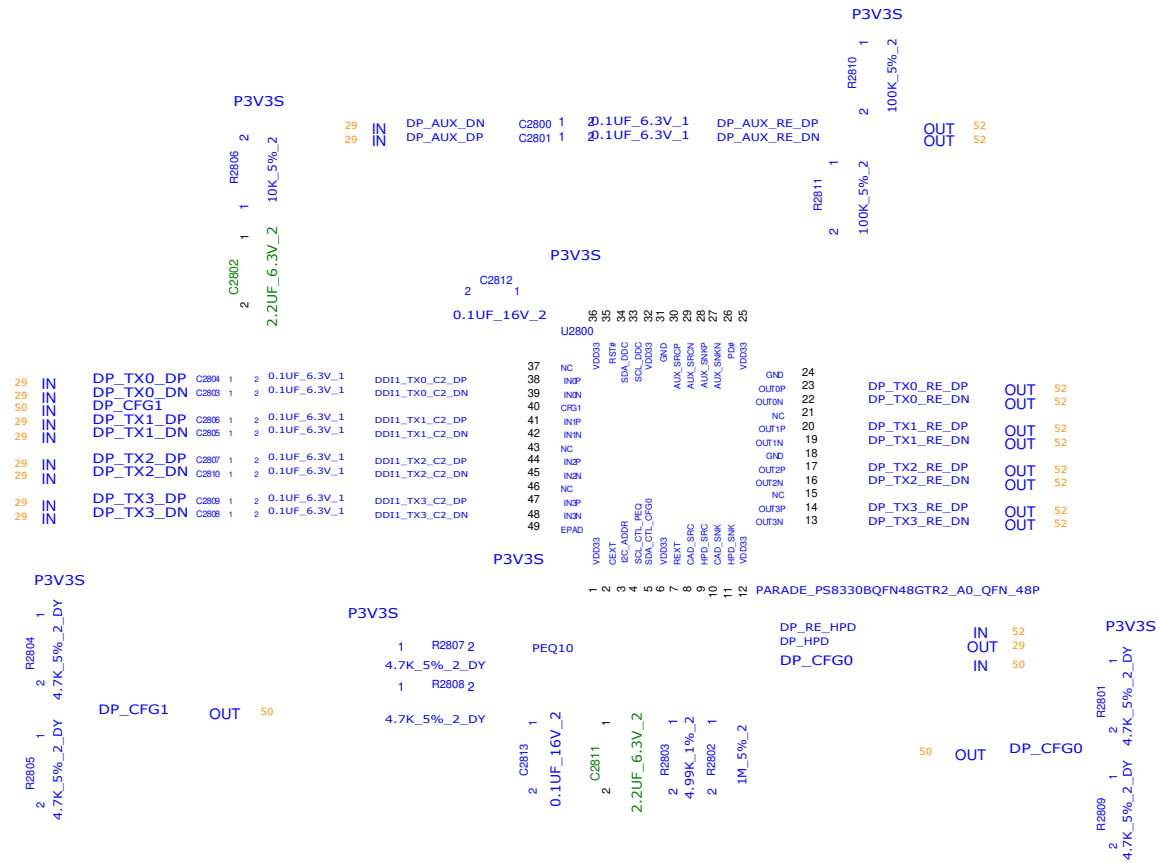
NGFF SSD1(PCIE/SATA 4X)

PCH AUTO SWAP DN/DP WHEN PCIE INTERFACE



INVENTEC

DP REDRIVER



INVENTEC

TITLE
A10 Block Diagram
DOC NUMBER
1310xxxxx-0-0
REV
X01

CHANGE by
PCB P/N XXXX
60xxxxxxxxxx

DATE
PCB VER 12-Apr-2019
X01

SIZE
A3
CODE
CS
SHEET 50 of 70

1

USB3 REDRIVER

REFERENCE 2600~2699(USB RESERVE)

D

D

C

C

B

B

A

A

INVENTEC



F

E

D

C

B

A

F

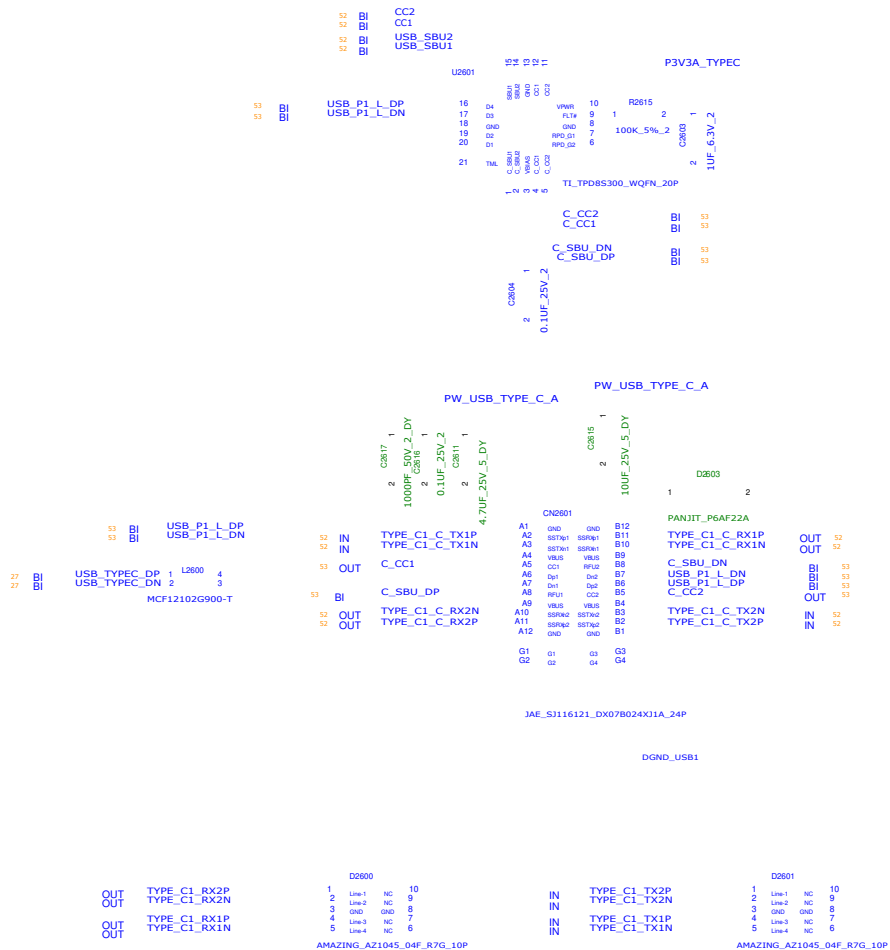
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D

C

B

A



INVENTEC

TITLE A10
SIZE C
CODE C3
SHEET 53
OCC NUMBER 1310xxxxxx-0-0
REV X01

CHANGE by XXX 60xxxxxxxxxx
DATE 12-Apr-2019
PCB VER X01

EDP CONN

D

C

B

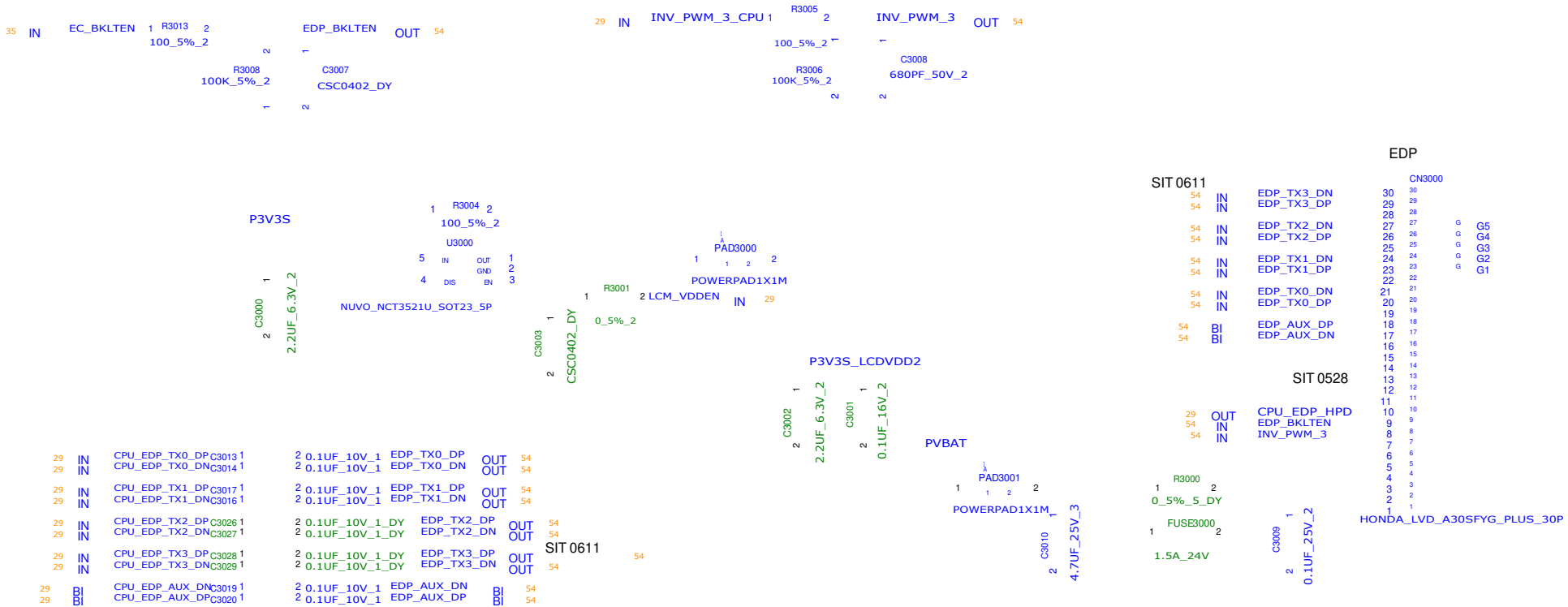
A

D

C

B

A



INVENTEC

D



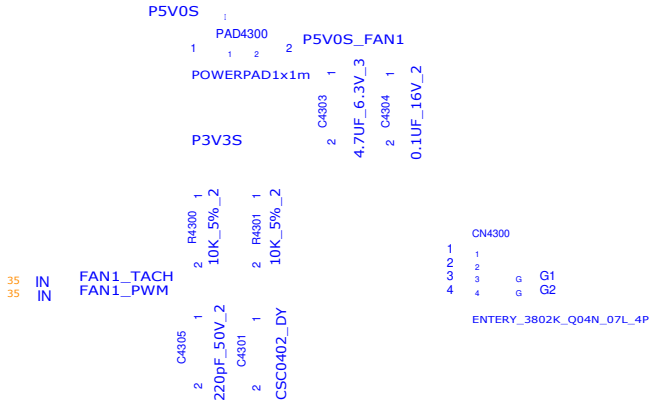
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B



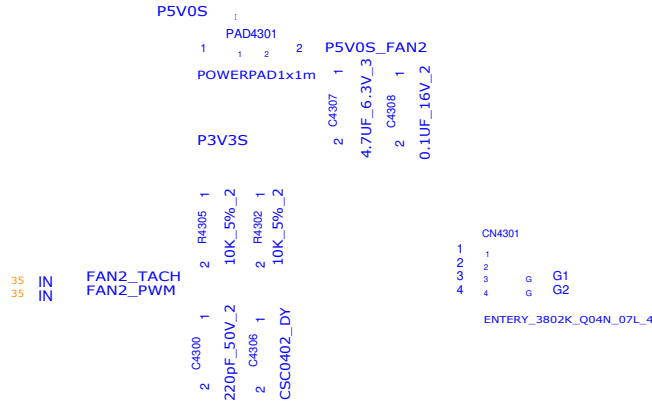
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C

FAN1 CN CPU

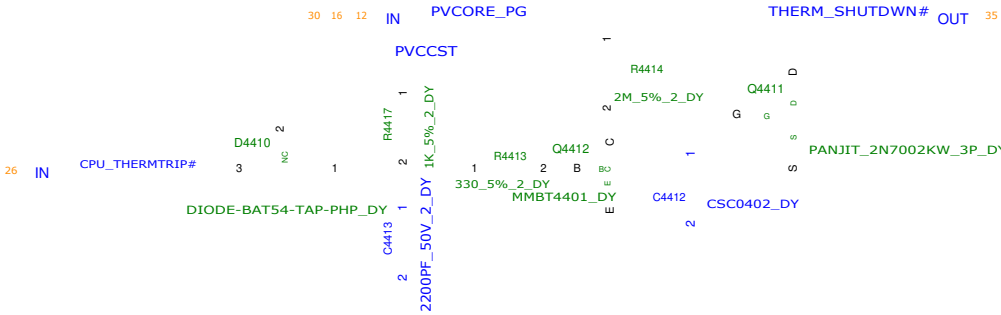
D



C

FAN2 CN CPU

B

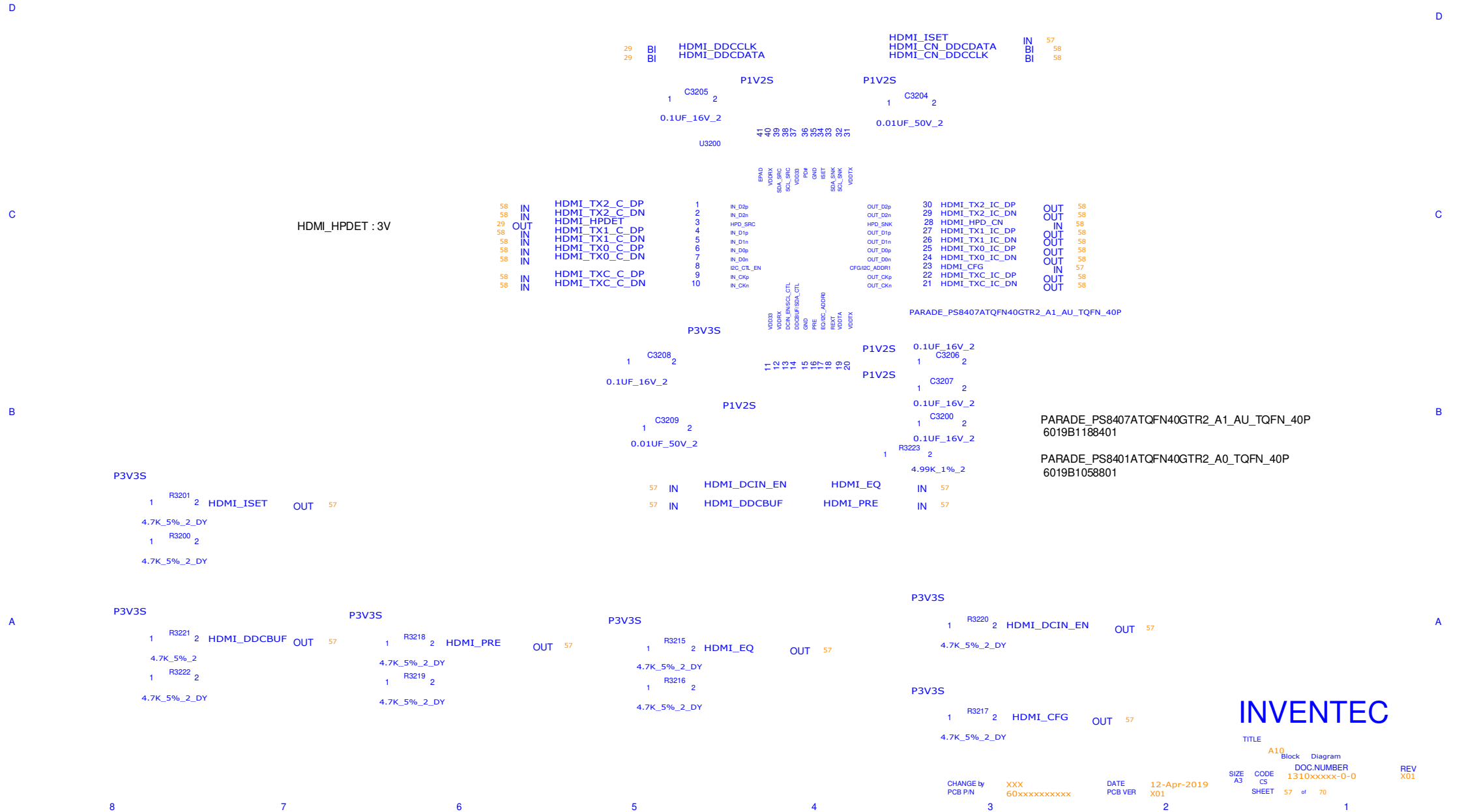


B

A

REFERENCE NUMBER:4411~4449

HDMI REPEATER (4K2K)



INVENTEC

TITLE
A10 Block Diagram
SIZE CODE DOC.NUMBER REV
A3 CS 1310xxxxx-0-0 X01
SHEET 57 of 70

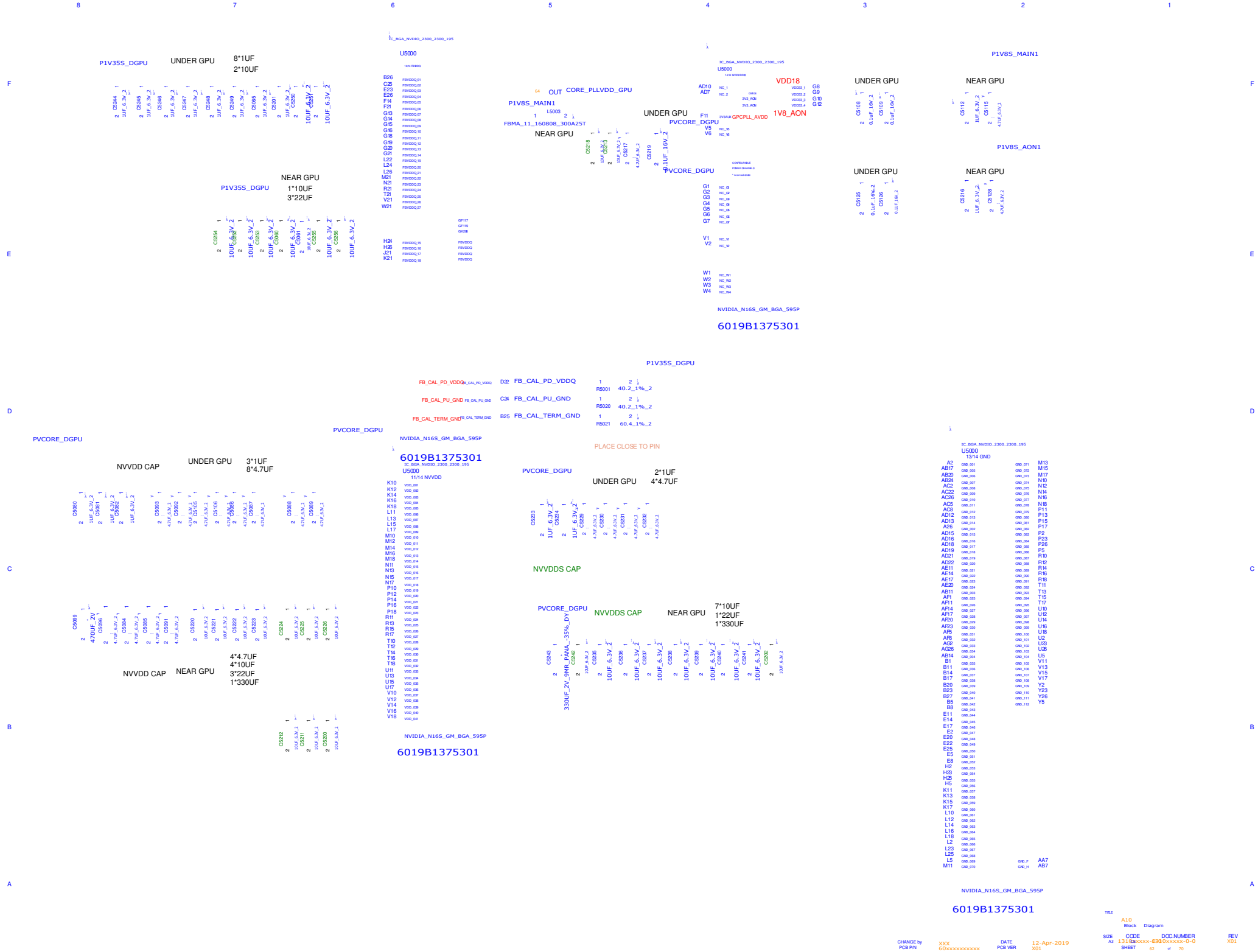


N17S-G0/G2

GDDR5 23X23

2019.10.03





MEMORY: FBA Partition 31..0
MEMORY: FBA Partition 63..32

M3=U5500
NON MIRROR

U5500

PIV355_DGPU

M4=U5501
MIRROR

U5501

PIV355_DGPU

INVENTEC

A



TITLE
A10 Block Diagram
SIZE CODE DOC.NUMBER
A3 CS 1310xxxxx-0-0
SHEET 66 of 70

12-Apr-2019
X01

D

D

C

C

B

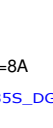
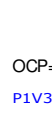
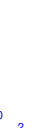
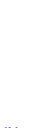
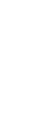
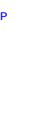
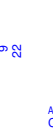
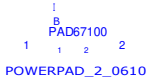
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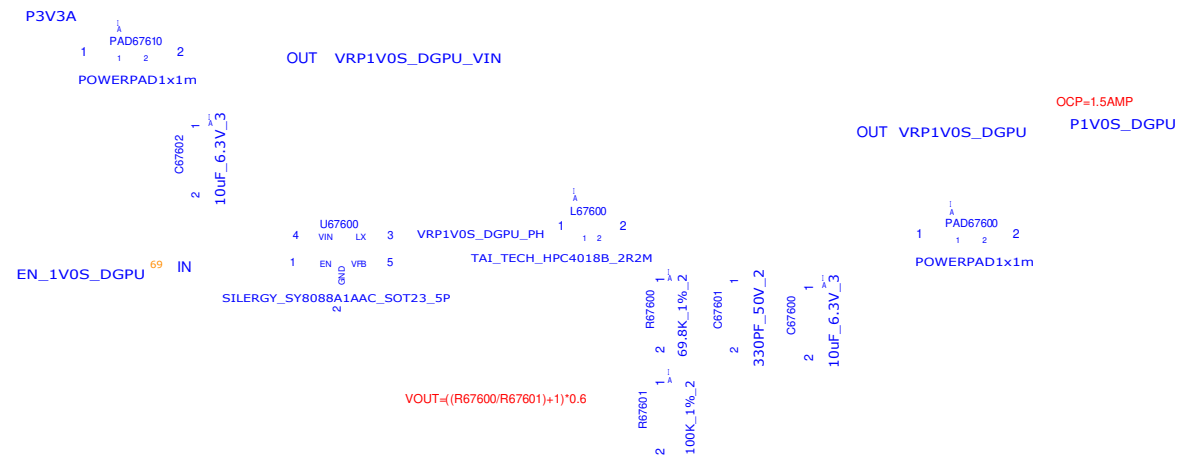
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PVBAT



INVENTEC



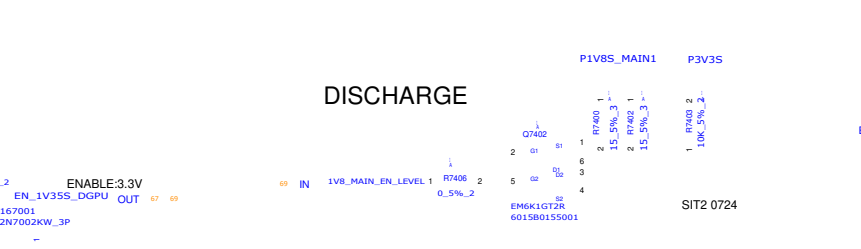
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A10 Block Diagram
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REV
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A3 CS 1310xxxxx-0-0
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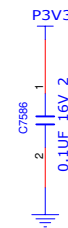
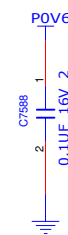
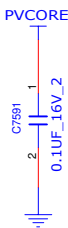
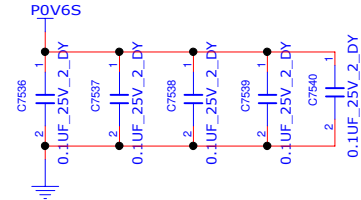
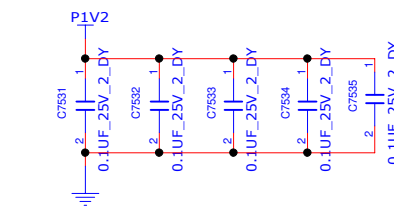
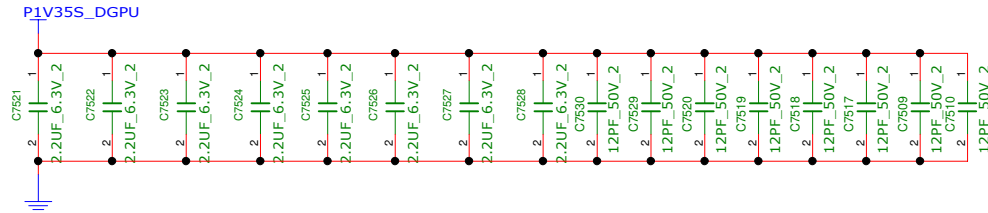
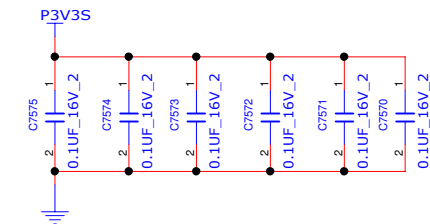
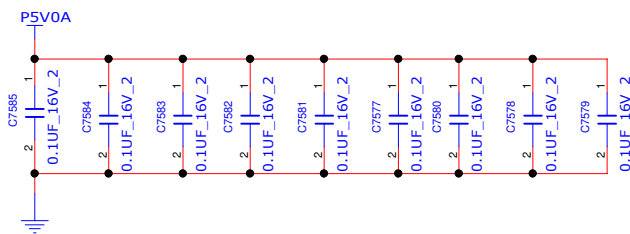
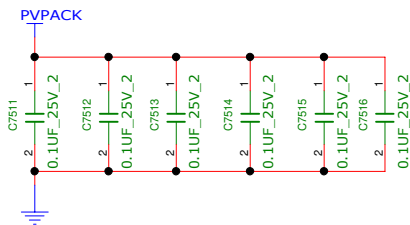
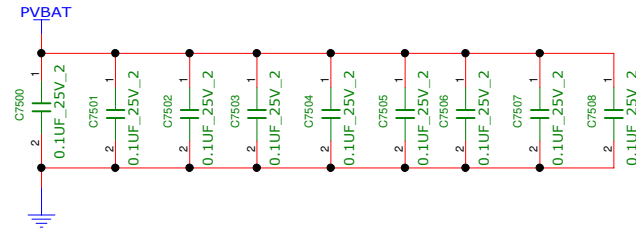
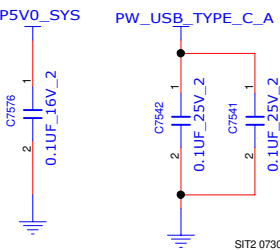
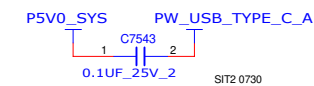
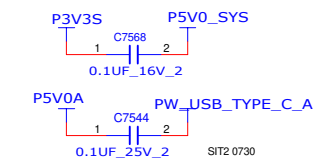
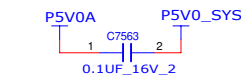
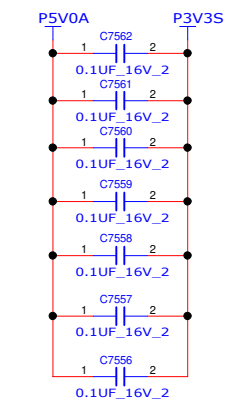
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A10 Block Diagram			
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CHANGE by	XXX	DATE	12-Apr-2019
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